PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Wood et al.

Serial No.: 10/666,742

Filed: September 19, 2003

For: METHODS FOR THINNING SEMICONDUCTOR SUBSTRATES THAT EMPLOY SUPPORT STRUCTURES FORMED ON THE SUBSTRATES (Amended)

Confirmation No.: 6057

Examiner: A. Ghyka

Group Art Unit: 2812

Attorney Docket No.: 2269-6095US

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APPEAL BRIEF

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P.O. Box 1450
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Attn: Board of Patent Appeals and Interferences

Sirs:

This Appeal Brief is being submitted in the format required by 37 C.F.R. § 41.37(c)(1) and with the fee required by 37 C.F.R. § 41.20(b)(2).

(1) REAL PARTY IN INTEREST

U.S. Application Serial No. 10/666,742 (hereinafter "the '742 Application"), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter "the Office") at Reel No. 015025, Frame No. 0337. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

(2) RELATED APPEALS AND INTERFERENCES

There are currently no related appeals, interferences, or other actions of which appellants or their attorneys are aware that may have a bearing on the outcome of the decision of the Board of Patent Appeals and Interferences in the above-referenced appeal.

(3) STATUS OF CLAIMS

There are currently forty-five (45) claims pending and under consideration in the '742 Application.

The '742 Application was filed with sixty-nine (69) claims. Claims 70-98 were subsequently added. Claims 17-20, 23-34, and 70-98 are currently pending and under consideration in the '742 Application.

Claims 17-20 and 23-34 have been allowed, and claims 75 and 87 are drawn to allowable subject matter.

Final rejections have been presented against claims 70-74, 76-86, and 88-98. The final rejections of claims 70-74, 76-86, and 88-98 are the subject of this appeal.

(4) STATUS OF AMENDMENTS

A final Office Action was mailed on October 10, 2007. No amendments have since been presented in the '742 Application.

(5) SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 70 is drawn to a process that requires "***molding*** a support structure [40'] on an active surface of [a] semiconductor substrate [10]..." (emphasis supplied). FIGs. 12A and 12B; page 19, lines 4-24 (paragraphs **[0088]** through **[0091]**). In addition, the method of independent claim 70 includes "removing material from a back side [16] of the semiconductor substrate [10] to form a thinned semiconductor substrate [10'']" (FIGs. 14A and 14B; page 20, line 29, to page 21, line 30 (paragraphs **[0096]** through **[0099]**)) and "transporting the thinned semiconductor substrate [10''] for further processing" (FIG. 15; page 22, lines 1-12 (paragraphs **[00100]** and **[00101]**)).

Independent claim 82 is drawn to a substrate thinning process (*e.g.*, backgrinding). The substrate thinning process of independent claim 82 includes securing a semiconductor substrate to a platen. FIG. 14A; page 21, lines 6-15 (paragraph **[0097]**). An active surface 12 of the semiconductor substrate 10 faces the platen 400, with a support structure 40 on the active surface abutting either the platen 400 or a feature 412 on the platen 400. *Id.* Once the semiconductor substrate 10 is secured to the platen 400 in this manner, material is removed from its back side 16. FIG. 14B; page 21, lines 16-27 (paragraph **[0098]**). The thinned semiconductor

substrate 10″ may then be transported for further processing. FIG. 15; page 22, lines 1-12 (paragraphs **[00100]** and **[00101]**).

(6) GROUND OF REJECTION TO BE REVIEWED ON APPEAL

The 35 U.S.C. § 103(a) rejection of claims 70-74, 76-86, and 88-98 for being drawn to subject matter that is allegedly unpatentable over the subject matter taught in U.S. Patent 5,354,695 to Leedy et al. (hereinafter "Leedy"), in view of teachings from U.S. Patent 6,562,661 to Grigg (hereinafter "Grigg") and U.S. Patent 6,524,881 to Tandy et al. (hereinafter "Tandy").

(7) ARGUMENT

(A) APPLICABLE LAW

There are several requirements in establishing a *prima facie* case of obviousness against the claims of a patent application. All of the limitations of the claim must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 985 (CCPA 1974); *see also* MPEP § 2143.03. Even then, a claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR Int'l Co. v. Teleflex Inc.*, 82 USPQ2d 1396 (2007). The Office must also establish that one of ordinary skill in the art would have had a reasonable expectation of success that the purported modification or combination of reference teachings would have been successful. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). There must also be "an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR* at 1396. That reason must be found in the prior art, common

knowledge, or derived from the nature of the problem itself, and not based on the Applicant's disclosure. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1367 (Fed. Cir. 2006). A mere conclusory statement that one of ordinary skill in the art would have been motivated to combine or modify reference teachings will not suffice. *KSR* at 1396.

(B) ART RELIED UPON

Leedy

In the process that has been disclosed in Leedy, a preformed structure is secured to an active surface of a substrate. Col. 8, lines 48-52; FIG. 1f.

Grigg

The teachings of Grigg are limited to use of so-called "stereolithography" processes to fabricate stiffeners on a tape substrate.

Tandy

The teachings of Tandy relate to a process by which a laser-markable tape is secured to the backside 12 of a wafer 10. Fig. 4A; col. 6, lines 44-49.

(C) ANALYSIS

It is respectfully submitted that there are at least two reasons that a *prima facie* case of obviousness has not been established against any of claims 70-74, 76-86, and 88-98.

It is respectfully submitted that the Examiner has erred in at least one respect: no apparent reason has been provided as to why one of ordinary skill in the art would have combined teachings from Leedy, Grigg, and Tandy to provide a process in which a support structure is molded onto an active surface of a semiconductor substrate.

Independent claim 70 is drawn to a process that requires "***molding*** a support structure on an active surface of [a] semiconductor substrate..." (emphasis supplied).

It is respectfully submitted that, since none of Leedy, Grigg, or Tandy teaches or suggests a process that includes molding, there would have been no apparent reason for one of ordinary skill in the art to combine teachings from these references to develop a method in which a support structure is molded.

Moreover, it is respectfully submitted that, without the benefit of hindsight that the above-referenced application has provided to the Examiner, there would have been no apparent reason for one of ordinary skill in the art to combine teachings from Leedy, Grigg, and Tandy in such a way as to render obvious the subject matter recited in independent claim 70, nor has the Examiner provided a convincing line of reasoning as to why one of ordinary skill in the art would have had any apparent reason to combine teachings from these references in the manner that has been asserted.

It has been asserted that "all of the references pertain to making semiconductors..." Final Office Action, page 7. This assertion overlooks the fact that "making semiconductors" is a broad field that includes a large number of separate and distinct processes that employ different techniques. In combining teachings from Leedy, Grigg, and Tandy, the Examiner has attempted

to combine teachings from separate fields within the general field of "making semiconductors": thinning; the manufacture of flexible carrier substrates; and wafer marking, respectively.

Even overlooking the fact that the three cited references pertain to three different fields, it is respectfully submitted that one of ordinary skill in the art wouldn't have been motivated to combine their teachings to develop the method recited in independent claim 70 since none of the cited references teaches or suggests "molding" a support structure.

Therefore, the teachings of Leedy, Grigg, and Tandy do not support a *prima facie* case of obviousness against the subject matter to which independent claim 70 is drawn. As such, under 35 U.S.C. § 103(a), the subject matter to which independent claim 70 is drawn is allowable over the teachings of Leedy, Grigg, and Tandy.

Claims 71-74 and 76-81 are each allowable, among other reasons, for depending directly or indirectly from independent claim 70, which is allowable.

The substrate thinning (*e.g.,* backgrinding) process of independent claim 82 includes securing a semiconductor substrate to a platen. An active surface of the semiconductor substrate must face the platen, with a support structure on the active surface abutting either the platen or a feature on the platen. Once the semiconductor substrate is secured to the platen in this manner, material is removed from its back side.

The process of Leedy includes the *formation of a frame* 18 *while the substrate* 10 *is thinned.* Col. 7, line 17, to col. 8, line 14; Figs. 1a and 1b. Thus, the frame 18, which is on the back side of the substrate 10 (col. 7, lines 51-52; Figs. 1a and 1b), could not abut a platen or a feature on the platen during thinning of the substrate 10. While Leedy teaches that a *separate*

bonding frame or ring 19 may be *secured* to an active surface of the substrate 10, the teachings of Leedy are limited to securing the bonding frame or ring 19 to the active surface of the substrate 10 *after the substrate* 10 *has been thinned.* Col. 8, lines 48-52. Thus, Leedy does not teach or suggest removing material from the back side of a substrate while a support structure on the active surface of the substrate abuts a platen or a feature on a platen, as is required of the method of independent claim 82.

Grigg includes no teaching or suggestion that material may be removed from either side of the flexible substrate disclosed therein, let alone that material may be removed as a support structure on one surface of the flexible substrate abuts a platen or a feature on the platen.

The teachings of Tandy that relate to the removal of material from the back side of a semiconductor wafer are limited to securing a front side of the wafer 10 to a platen 56, which provide physical support for the wafer 10 as a grinding wheel 52 removes material from the back side of the wafer 10. Col. 5, lines 30-34; FIG. 2. Tandy does not teach or suggest that a support structure of any type is secured to the front side of the wafer 10, between the wafer 10 and the platen 56, during the backgrinding process. Therefore, Tandy does not teach or suggest that material may be removed from the wafer 10 while a support structure on the front side of the wafer abuts the platen 56 or a feature on the platen 56, as required by independent claim 82.

Therefore, it is evident that none of Leedy, Grigg, or Tandy teaches or suggests the element of independent claim 82 requiring that a support structure on an active surface of a substrate abut a platen or a feature on the platen as material is removed from the back side of the substrate.

Moreover, since none of Leedy, Grigg, or Tandy identifies any shortcomings with the wafer thinning processes of Leedy and Tandy, and since the Examiner has not identified any problems with these processes, or with any other support for the assertion that one of ordinary skill in the art would have been motivated to support a wafer before material is removed from the wafer (*e.g.*, in the manner recited in independent claim 82), it is respectfully submitted that without the benefit of hindsight, one of ordinary skill in the art wouldn't have had any apparent reason to combine teachings from Leedy, Grigg, and Tandy in the manner that has been asserted by the Examiner.

In view of the foregoing, it is respectfully submitted that the Examiner has not established a *prima facie* case of obviousness against the subject matter recited in independent claim 82, or in any of claims 83-86 or 88-98 depending therefrom, as would be required to maintain the 35 U.S.C. § 103(a) rejections of these claims.

It is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 70-74, 76-86, and 88-98 be withdrawn, and that each of these claims be allowed.

8. CLAIMS APPENDIX

The current status of each claim that has been introduced into the '742 Application is set forth in CLAIMS APPENDIX to this Appeal Brief.

9. EVIDENCE APPENDIX

There is no EVIDENCE APPENDIX to this Appeal Brief.

10. RELATED PROCEEDINGS APPENDIX

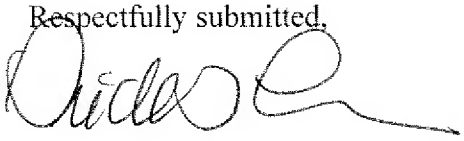
There is no RELATED PROCEEDINGS INDEX to this Appeal Brief.

11. CONCLUSION

It is respectfully submitted that, under 35 U.S.C. § 103(a), each of claims 70-74, 76-86, and 88-98 is drawn to subject matter that is patentable over the subject matter taught in Leedy, in view of teachings from Grigg and Tandy.

Accordingly, reversal of the 35 U.S.C. § 103(a) rejections of claims 70-74, 76-86, and 88-98 is respectfully solicited, as is the allowance of each of these claims.

Respectfully submitted,



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CLAIMS APPENDIX

17. A method for thinning a semiconductor substrate, comprising:

forming a support structure on an active surface of the semiconductor substrate such that the support structure includes an outer peripheral portion that extends beyond an outer peripheral edge of the semiconductor substrate and a downwardly extending portion located laterally adjacent to the outer peripheral edge of the semiconductor substrate;

removing material from a back side of the semiconductor substrate to form a thinned semiconductor substrate; and

transporting the thinned semiconductor substrate for further processing.

18. The method of claim 17, wherein forming the support structure comprises forming a support ring on the active surface adjacent to an outer peripheral edge of the semiconductor substrate.

19. The method of claim 18, wherein forming the support ring comprises forming the support ring such that each semiconductor device that has been fabricated on the active surface is located within an inner periphery of the support ring and is exposed therethrough.

20. The method of claim 17, wherein forming the support structure includes forming a layer of packaging material over the active surface and extending radially outward to at least an outer peripheral edge of the semiconductor substrate.

23. The method of claim 17, wherein forming the support structure comprises:

forming a layer comprising unconsolidated material over at least an outer peripheral portion of the active surface; and

at least partially consolidating the unconsolidated material within at least outer peripheral regions of the layer.

24. The method of claim 23, wherein at least partially consolidated the unconsolidated material comprises directing a focused energy beam onto at least the outer peripheral regions of the layer.

25. The method of claim 24, wherein directing the focused energy beam comprises directing a laser beam onto at least the outer peripheral regions of the layer.

26. The method of claim 17, wherein forming the support structure comprises stereolithographically forming the support structure.

27. The method of claim 17, wherein forming the support structure comprises:

positioning a preformed film of support material over the active surface; and

removing selected regions of the preformed film.

28. The method of claim 17, wherein forming the support structure comprises molding the support structure on the active surface.

29. The method of claim 17, further comprising:

securing the semiconductor substrate to a platen with the active surface facing the platen and the support structure abutting at least one surface or feature of or on the platen.

30. The method of claim 29, wherein securing the semiconductor substrate comprises applying a negative pressure to the active surface.

31. The method of claim 29, wherein securing the semiconductor substrate includes sealing the support structure against the at least one surface or feature.

32. The method of claim 17, wherein removing material from the back side of the semiconductor substrate comprises at least one of chemically and mechanically removing material from the back side.

33. The method of claim 17, wherein removing material from the back side of the semiconductor substrate comprises back grinding.

34. The method of claim 17, wherein the support structure supports the thinned semiconductor substrate during transporting thereof.

70. A method for thinning a semiconductor substrate, comprising:

molding a support structure on an active surface of the semiconductor substrate;

removing material from a back side of the semiconductor substrate to form a thinned semiconductor substrate; and

transporting the thinned semiconductor substrate for further processing.

71. The method of claim 70, wherein forming the support structure comprises forming a support ring on the active surface adjacent to an outer peripheral edge of the semiconductor substrate.

72. The method of claim 71, wherein forming the support ring comprises forming the support ring such that each semiconductor device that has been fabricated on the active surface is located within an inner periphery of the support ring and is exposed therethrough.

73. The method of claim 70, wherein forming the support structure includes forming a layer of packaging material over the active surface and extending radially outward to at least an outer peripheral edge of the semiconductor substrate.

74. The method of claim 70, wherein forming the support structure comprises forming the support structure to include an outer peripheral portion that extends beyond an outer peripheral edge of the semiconductor substrate.

75. The method of claim 74, wherein forming the support structure further comprises forming the outer peripheral portion to include a downwardly extending portion located laterally adjacent to the outer peripheral edge of the semiconductor substrate.

76. The method of claim 70, further comprising:

securing the semiconductor substrate to a platen with the active surface facing the platen and the support structure abutting at least one surface or feature of or on the platen.

77. The method of claim 76, wherein securing the semiconductor substrate comprises applying a negative pressure to the active surface.

78. The method of claim 76, wherein securing the semiconductor substrate includes sealing the support structure against the at least one surface or feature.

79. The method of claim 70, wherein removing material from the back side of the semiconductor substrate comprises at least one of chemically and mechanically removing material from the back side.

80. The method of claim 70, wherein removing material from the back side of the semiconductor substrate comprises back grinding.

81. The method of claim 70, wherein the support structure supports the thinned semiconductor substrate during transporting thereof.

82. A method for thinning a semiconductor substrate, comprising:

forming a support structure on an active surface of the semiconductor substrate;

securing the semiconductor substrate to a platen with the active surface facing the platen and the support structure abutting at least one surface or feature of or on the platen;

removing material from a back side of the semiconductor substrate supported by the support structure and the platen to form a thinned semiconductor substrate; and

transporting the thinned semiconductor substrate for further processing.

83. The method of claim 82, wherein forming the support structure comprises forming a support ring on the active surface adjacent to an outer peripheral edge of the semiconductor substrate.

84. The method of claim 83, wherein forming the support ring comprises forming the support ring such that each semiconductor device that has been fabricated on the active surface is located within an inner periphery of the support ring and is exposed therethrough.

85. The method of claim 82, wherein forming the support structure includes forming a layer of packaging material over the active surface and extending radially outward to at least an outer peripheral edge of the semiconductor substrate.

86. The method of claim 82, wherein forming the support structure comprises forming the support structure to include an outer peripheral portion that extends beyond an outer peripheral edge of the semiconductor substrate.

87. The method of claim 86, wherein forming the support structure further comprises forming the outer peripheral portion to include a downwardly extending portion located laterally adjacent to the outer peripheral edge of the semiconductor substrate.

88. The method of claim 82, wherein forming the support structure comprises:

forming a layer comprising unconsolidated material over at least an outer peripheral portion of the active surface; and

at least partially consolidating the unconsolidated material within at least outer peripheral regions of the layer.

89. The method of claim 88, wherein at least partially consolidated the unconsolidated material comprises directing a focused energy beam onto at least the outer peripheral regions of the layer.

90. The method of claim 89, wherein directing the focused energy beam comprises directing a laser beam onto at least the outer peripheral regions of the layer.

91. The method of claim 82, wherein forming the support structure comprises stereolithographically forming the support structure.

92. The method of claim 82, wherein forming the support structure comprises:
positioning a preformed film of support material over the active surface; and
removing selected regions of the preformed film.

93. The method of claim 82, wherein forming the support structure comprises molding the support structure on the active surface.

94. The method of claim 82, wherein securing the semiconductor substrate comprises applying a negative pressure to the active surface.

95. The method of claim 82, wherein securing the semiconductor substrate includes sealing the support structure against the at least one surface or feature.

96. The method of claim 82, wherein removing material from the back side of the semiconductor substrate comprises at least one of chemically and mechanically removing material from the back side.

97. The method of claim 82, wherein removing material from the back side of the semiconductor substrate comprises back grinding.

98. The method of claim 82, wherein the support structure supports the thinned semiconductor substrate during transporting thereof.

EVIDENCE APPENDIX

NONE

RELATED PROCEEDINGS APPENDIX

NONE